TSUNG-HAN LU

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WORK & PROFESSIONAL EXPERIENCE

PhD Researcher | San Diego, CA Sept.2024~Present

University of California, San Diego

- Specialized in **hardware-software co-design** for algorithm acceleration, achieving a 18.7x performance speedup and a 3200x reduction in energy consumption compared to a A100 GPU.
- Led the design and implementation of 3DDRAM for **hardware accelerator** to **Transformer** models, focusing on optimizing performance and power efficiency for **AI** workloads.

-Hardware Accelerator Design for Transformer Attention Mechanism Jan.2025~Mar.2025

- Designed and implemented a single-core 1-D vector processor for **Transformer acceleration**, achieving a total power of 242.4 mW and an area of 195,456 μm² post-PnR.
- Researched and evaluated two distinct architectures, a **1-D Vector Processor and a 2-D Systolic Array** , for accelerating the matrix multiplication between Query (Q) and Key (K) vectors.
- Scaled the architecture up to a 4-core version using a handshaking protocol and improved timing (WNS) by applying a 3-cycle multi-cycle path constraint.

-Machine Learning for Algorithmic Music Composition Mar.2025~Jun.2025

- Developed two distinct machine learning models for algorithmic music generation, encompassing the entire **ML** pipeline from data processing to evaluation.
- Implemented both symbolic generation models and continuous generation models.

-Digital VLSI Implementation of an Adder (RTL-to-GDSII) Mar.2025~Jun.2025

- Improved energy efficiency significantly, demonstrating over **40x less power consumption** compared to a standard Ripple-Carry Adder.
- Optimized the design by creating a custom full adder cell at the transistor level, contributing to a final energy-per-operation of only 2.805 fJ.

R&D process engineer (Chemical mechanical polish) | Hsinchu, Taiwan Nov.2021~Jul.2024

Taiwan Semiconductor Manufacturing Company (TSMC)

- Leaded the **N3/N3B** tech middle-of-line (MEOL) CMP team, achieving a 14% yield enhancement.
- Optimized **N2** front-end-of-line **(FEOL)**/ middle-of-line **(MEOL)** process flow.
- Minimized CMP defects by 92% and orchestrated CMP self-quality control measures.

EDUCATION

University of California, San Diego, La Jolla, CA Sept.2024~Present

PhD. in Electric and Computer Engineering.

National Tsing Hua University, Hsinchu, Taiwan Sept. 2019~Sept. 2021

Master of Science in Power Mechanical Engineering (GPA: 3.9).

Taipei Medical University, Taipei, Taiwan Jun. 2015~Jun. 2019

Bachelor of Science in Oral hygiene. (GPA: 3.54)

SKILLS

Programming Languages: System Verilog, MATLAB, Python

Skillset: Cadence Virtuoso, VLSI, Modelsim, Spectre, Cadence Genus, Cadence Innovus, AutoCAD, SolidWorks, Machine Learning, Dynamic Programming, Digital Circuit Design, Memory Acceleration, DRAM